R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

CLAIM AMENDMENTS

Support for the amendments to the claims can be found in the drawings as originally filed, for example, FIGS. 1-3 and in the specification as originally filed, for example, on page 5, line 20 through page 7, line 18, on page 12, line 12 through page 13, line 2 and on page 13, line 12 through page 14, line 6. As such, no new matter has been added.

CLAIM REJECTIONS UNDER 35 U.S.C. §112

The rejection of claims 2 and 5 under 35 U.S.C. §112, second paragraph, is respectfully traversed and should be withdrawn.

Claim 2 recites that the "one or more logic circuits comprises variable width logic circuits." One skilled in the art reading claim 2 in light of the specification would be appraised of the scope of the claimed invention. Specifically, the specification provides a number of examples of implementing variable width logic circuits (see page 11, line 21 through page 13, line 11). In one example, the specification provides:

> The circuit 100 may provide an architecture for implementing configurable hard cyclic redundancy check (CRC) functionality of varying width in a PLD. **Additionally, the circuit 100 may provide hard wired logic functionality of varying width.** In one example, the circuit 100 may be implemented as a programmable logic configured as a variable width multiplier. In another example, the circuit 100 may be implemented as a hard wired, dedicated logic block. For example, the hard wired dedicated logic block may be implemented as a hard multiplier block on silicon (e.g., not composed of programmable elements) (page 8, lines 10-19 of the specification, emphasis added).

In another example, the specification provides:

> However, the circuit 200 may be implemented to provide a varying number and/or widths of multipliers. For example, the circuit 200 may be implemented with a number of 8-bit hard wired multipliers. The 8-bit hard wired multipliers 202a-202n may be configured as:
> an 8-bit multiplier;
> an 16-bit multiplier (e.g., using four 8 x 8 bit multipliers);
> an 24-bit multiplier (e.g., using nine 8 x 8 bit multipliers); and
> an 32-bit multiplier (e.g., using sixteen 8 x 8 bit multipliers) (See page 12, line 12 through page 13, line 2 of the specification).

The specification also provides:

> The hard wired 8-bit or any size multipliers 202a-202n may be connected, in one example, by a routable interconnect (e.g., a programmable interconnect matrix, not shown). The routable interconnect may link function blocks (e.g., the multipliers 202a-202n and the adder 204).
>
> Additionally, the routable interconnect may allow the 8-bit hard wired multipliers 202a-

> 202n to be configured as a number of **variable width multipliers**. The signals SHIFTa-SHIFTn may allow addition of the partial products created by the multiply function (e.g., the signals MULTIa-MULTIn) (see page 13, lines 3-11 of the specification, emphasis added).

Because claim 2 when read in the light of the specification would appraise one skilled in the art of the scope of the invention, claim 2 is neither vague nor indefinite and the rejection should be withdrawn.

Claim 5 recites that "one or more of the logic circuits **comprises** a hard wired multiplier." The interpretation of the claim language as meaning "the logic circuit is hard wired" is not technically correct (see page 2, second paragraph of section no. 2 of the Office Action). The term "comprises" is a term of art that is inclusive or open-ended and does not exclude additional, unrecited elements or method steps (MPEP §2111.03). Therefore, stating that a logic circuit comprises a hard wired element does not preclude the logic circuit from being programmable as urged in the Office Action (see page 2, second paragraph of section no. 2 of the Office Action). As such, the rejection of Claim 5 as being vague and indefinite does not appear to be proper and should be withdrawn.

Furthermore, Claim 1, from which Claim 5 depends, recites one or more logic circuits configured to provide logical operation

wherein the one or more logic circuits comprise (i) **programmable logic elements** and (ii) **non-programmable logic elements** within a programmable logic device. Taking the hard wired multiplier as the non-programmable logic element (as suggested on page 2, second paragraph of section no. 2 of the Office Action), the presently claimed logic circuit also comprises **programmable logic elements**. Therefore, the rejection of Claim 5 as being "vague and indefinite because if the logic circuit are [sic: is] hard wired, then the circuit can't be programmable" (as recited on page 2, second paragraph of section no. 2 of the Office Action) does not appear to be proper. As such, the rejection should be withdrawn.

Furthermore, Claim 5 when read in the light of the specification would reasonably apprise one of skill in the art of the scope of the invention. Specifically, in one example, the specification provides:

> The circuit 100 may illustrate **a single hard wired multiplier**. However, the circuit 100 may implement another appropriate number of hard wired multipliers (to be described in connection with FIG. 2). Additionally, the hard wired multiplier 100 may be implemented with any appropriate width and/or depth in order to meet the criteria of a particular implementation. For example, the circuit 100 may be implemented with **a number of 8-bit hard wired multipliers**. (page 9, line 3-10 of the specification, emphasis added)

In another example, the specification provides:

> The hard wired 8-bit or any size multipliers 202a-202n may be connected, in one example, by a routable interconnect (e.g., a programmable interconnect matrix, not shown). The routable interconnect may link function blocks (e.g., the multipliers 202a-202n and the adder 204). Additionally, the routable interconnect may allow the 8-bit hard wired multipliers 202a-202n to be configured as a number of **variable width multipliers**. The signals SHIFTa-SHIFTn may allow addition of the partial products created by the multiply function (e.g., the signals MULTIa-MULTIn) (see page 13, lines 3-11 of the specification, emphasis added).

Because claim 5 would appraise one skilled in the art of the scope of the invention when read in the light of the specification, claim 5 is neither vague nor indefinite and the rejection should be withdrawn.

Furthermore, one skilled in the art would understand that the non-programmable logic elements recited in claim 1 are fully consistent with the recitation in claim 5 that the one or more logic circuits comprises a hardwired multiplier. As such, the recitation of claim 5 is clear and definite and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-5, 7-13 and 15-22 under 35 U.S.C. §102(b) as being anticipated by New '834 (hereinafter New) is respectfully traversed and should be withdrawn.

New is directed to a field programmable gate array with distributed gate array functionality (Title).

In contrast, the presently claimed invention (claim 1) provides one or more logic circuits configured to provide logical operation where the one or more logic circuits comprise programmable logic elements and **non-programmable logic elements** within a programmable logic device. Claims 15 and 16 include similar recitations. New does not disclose or suggest non-programmable logic elements, as presently claimed. Therefore, New does not disclose or suggest each and every element of the presently claimed invention arranged as in the present claims. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Specifically, the position taken in the Office Action that the a sea of gates (SOG) gate array of New is similar to the presently claimed non-programmable logic elements is not technically correct (see page 2, last two lines through page 3, line 4 of the Office Action). In particular, New discloses that although the sea of gates (SOG) gate arrays are a type of **non-field** programmable gate array (column 1, lines 39-41 of New), the sea of gates gate arrays are nevertheless **programmable**. For example, the Abstract of New provides:

> . . . The non-field programmable gate array can be used to provide a plurality of **mask-programmable** input/output driver circuits for connection to the pads of the FPGA (Abstract of New, emphasis added).

New further discloses that:

> In an SOG gate array, a predefined pattern of transistors are connected directly with user-defined metal [i.e., **mask-programmed**], both to form gates and to interconnect those gates (column 1, lines 45-47 of New).

Further reference is made by New to the programmability of the SOG gate arrays, for example, in column 2, lines 12-14:

> . . . a corresponding non-field programmable gate array, such as a **mask programmed** gate array, or more specifically a sea-of-gates (SOG) gate array (emphasis added);

in column 8, lines 16-18:

> As described in more detail below, the SOG gate array 601 can be **mask-programmed** to implement an input and/or output driver circuit 615 which is coupled to the I/O pad 602 (emphasis added);

and in column 8, lines 36-44:

> The SOG gate array 601 includes **logic elements which can be programmed** to vary the composition of the input buffer 621 and the output buffer 622 (emphasis added).

Since the sea of gates array of New are **programmable**, albeit by a mask, it follows that New does not disclose or suggest a **non-programmable** logic element, as presently claimed.

Furthermore, the Office Action does not present any evidence or line of reasoning why one of ordinary skill in the art would view a **mask-programmed** gate array as being the same as a **non-programmable** element, as presently claimed. In contrast to New, the present specification provides a hard wired multiplier as an example of a non-programmable logic element:

> The circuit 100 may provide an architecture for implementing configurable hard cyclic redundancy check (CRC) functionality of varying width in a PLD. Additionally, the circuit 100 may provide hard wired logic functionality of varying width. In one example, the circuit 100 may be implemented as a programmable logic configured as a variable width multiplier. In another example, the circuit 100 may be implemented as a hard wired, dedicated logic block. For example, the hard wired dedicated logic block may be implemented as a hard multiplier block on silicon (e.g., **not composed of programmable elements**) (page 8, lines 10-19 of the specification, emphasis added).

The Office Action admits that a hard wired circuit is not programmable:

> . . . if the logic circuit are [sic:is] hard wired, then the circuit can't be programmable. (page 2, section no. 2, second paragraph of the Office Action).

Because New discloses that a SOG gate array **includes logic elements which can be programmed** (column 8, lines 36-44), it follows that New does not disclose or suggest one or more logic circuits configured to provide logical operation, wherein the one or more

logic circuits comprise (i) programmable logic elements and (ii) **non-programmable logic elements** within a programmable logic device (PLD), as presently claimed. Therefore, New does not disclose or suggest each and every element of the presently claimed invention, arranged as in the present claims. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claims 2-14 and 17-22 depend, either directly or indirectly, from claims 1 and 16 which are believed to be allowable. New claims 23 and 24 depend, either directly or indirectly, from claim 1 which is believed to be allowable. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claim 6 under 35 U.S.C. §103(a) as being unpatentable over New '834 is respectfully traversed and should be withdrawn.

For the reasons presented above, New does not disclose or suggest each and every element of the presently pending claim 1. Specifically, New does not disclose or suggest non-programmable logic elements, as presently claimed. Therefore, presently pending claim 1 is fully patentable over New. Claim 6 depends directly

from claim 1 which is believed to be allowable. As such, claim 6 is fully patentable over the cited reference and the rejection should be withdrawn.

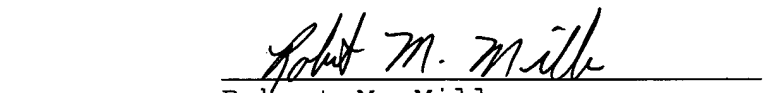
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicant's representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



Robert M. Miller
Registration No. 42,892
24025 Greater Mack, Suite 200
St. Clair Shores, MI 48080
(586) 498-0670

Dated: February 12, 2003

Docket No.: 0325.00361